Remarks

In view of the above amendments and the following remarks, reconsideration of the objection and rejections and further examination are requested.

The specification and abstract have been reviewed and revised to make a number of editorial revisions thereto. Further, the specification has been amended so as to address the objection thereto. A substitute specification and abstract including the revisions have been prepared and are submitted herewith. No new matter has been added. Also submitted herewith is a marked-up copy of the specification and abstract indicating the changes incorporated therein. As a result, withdrawal of the objection to the specification is respectfully requested.

Claims 1-8 and 15-26 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama (US 5,045,939) in view of Takabatake (US 6,320,909) and Stam (US 6,631,316). Claims 9 and 27-30 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama in view of Takabatake and Stam and further in view of Maze (US 4,573,080). Claims 10 and 31-34 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama in view of Takabatake and Stam and further in view of Eglit (US 6,054,980). Claim 11 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama in view of Stam. Claim 12 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Masuda (US 6,791,623) in view of Stam. Claim 13 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Masuda in view of Stam and further in view of Okayama. Claim 14 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Masuda in view of Stam and Okayama and further in view of Worrell (US 6,633,344).

Claims 1-5, 11, 12 and 14 have been amended so as to further distinguish the present invention, as recited in these claims, from the references relied upon in the above-mentioned rejections.

Further, claims 1-34 have been amended to make a number of editorial revisions thereto. These revisions have been made to place the claims in better U.S. form. None of these amendments have been made to narrow the scope of protection of the claims, or to address issues related to patentability, and therefore, these amendments should not be construed as limiting the scope of equivalents of the claimed features offered by the Doctrine of Equivalents.

The above-mentioned rejections are submitted to be inapplicable to the amended claims for the following reasons.

Claim 1 is patentable over the combination of Okayama, Takabatake and Stam, since claim 1 recites a clock conversion apparatus including, in part, a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period; a first counter circuit for counting a first clock, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written into the memory using at least a portion of the addresses of the memory a plurality of times; and a second counter circuit for counting a second clock, and generating read addresses of the memory so that the data corresponding to the predetermined period, which have been written in the memory, can be read from the memory using at least the portion of the addresses of the memory a plurality of times. The combination of Okayama, Takabatake and Stam fails to disclose or suggest the first counter circuit and the second counter circuit as recited in claim 1.

Okayama discloses an apparatus for converting a wide screen television signal into a normal screen television signal. The apparatus includes a line memory 25 which is sufficient for storing all samples of the digital wide screen television signal in one horizontal line. For a writing operation of the memory 25, the memory 25 receives at its write clock terminal a first clock signal CK1 and at its write address port a write address WA generated by a write address counter 27. The write address counter 27 counts up in response to the first clock signal CK1. Samples stored in the line memory 25 are read out by applying a second clock signal CK2 to a read clock terminal of the memory 25 and by applying read address RA to a read address port of the memory 25. The read address RA is generated by a read address counter 28 which counts up from a start address SA set at its preset terminal in response to the second clock signal CK2. The apparatus performs time axis expansion of the television signal by varying the frequencies of the first and second clock signals CK1 and CK2. (See column 3, lines 4-57 and Figure 2).

As discussed above, Okayama does disclose that the line memory 25 receives the first and second clock signals CK1 and CK2 for writing and reading data to/from the memory 25. However, as admitted in the rejection, Okayama fails to disclose or suggest that the memory 25 has a number of addresses that is less than a number of address required for storage of data corresponding to a predetermined period. Further, Okayama fails to disclose or suggest that the write address counter 27 and the read address counter 28 generate respective write and read addresses of the memory 25 so that data corresponding to a predetermined period can be written and read to/from the memory 25 using at least a portion of the addresses of the memory 25 a

plurality of times. As a result, Takabatake and/or Stam must disclose or suggest these features in order for the combination to render claim 1 obvious.

Regarding Takabatake, it is relied upon as disclosing a delay circuit 60 that delays a picture synchronization signal PSYNC, which is outputted from a control unit 14a, by a prescribed time, whereby a switching circuit 80 can selectively invalidate the delay provided by the delay circuit 60. (See column 22, lines 29-65). However, Takabatake fails to disclose or suggest the above-discussed features of claim 1.

Regarding Stam, it is relied upon as disclosing an image processing system that includes a memory 106 that has less memory than is needed to store all of the pixels of an image. As a result, only select pixels are stored in the memory 106. (See column 2, lines 18-23 and column 8, lines 44-61). However, while Stam does disclose that the memory 106 does not have enough capacity to store all of the pixels of an image, it is apparent that Stam fails to disclose or suggest the first and second counter circuits as recited in claim 1.

Since Takabatake and Stam fail to address all of the deficiencies of Okayama, it is apparent that the combination of Okayama, Takabatake and Stam fails to render claim 1 obvious. As a result, claim 1 is patentable over the combination of Okayama, Takabatake and Stam.

Further, (1) Maze, (2) Eglit, (3) Worrell, and (4) Masuda are relied upon as disclosing (1) a generating 28 having a detector 214 that supplies a reset pulse to a 10-bit address counter 202 to reset the counter 202 upon each transition of a signal R/W, (2) a comparator circuit 540 for comparing a last address generated by a write address counter 410 with a read address provided by a read address counter 440, and when the addresses are equal, generating a signal which resets the read address counter 440 to zero, (3) a memory management process for digital video data that is capable of detecting/buffering various video format schemes via a field type detector 78 located in a video input interface 12, and (4) an image display system including a video signal processor 2, a frequency resolution conversion circuit 4 and a video output circuit 5. However, it is apparent that none of these references discloses or suggests the above–discussed features of claim 1.

As for claims 2-5, 11, 12 and 14, they are patentable over the references relied upon in the rejections for reasons similar to those set forth above in support of claim 1. That is, claims 2-5, 11, 12 and 14 each recite that data corresponding to a predetermined period (or one horizontal line) is written to and/or read from a memory having a capacity less than the predetermined

period (or one horizontal line) using at least a portion of addresses of the memory a plurality of times, which features are not disclosed or suggested by the references.

Because of the above-mentioned distinctions, it is believed clear that claims 1-34 are allowable over the references relied upon in the rejections. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-34. Therefore, it is submitted that claims 1-34 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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